



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,637	06/30/2000	Jin Yang	42390.P9429	9275

8791 7590 12/07/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER

CRAIG, DWIN M

ART UNIT

PAPER NUMBER

2123

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/608,637

Applicant(s)

YANG, JIN

Examiner

Dwin M. Craig

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 September 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 4,5,8,14-18,28 and 31-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 4, 5, 8,14-18, 28 and 31-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/28/06 has been entered.

1.1 Claims 4, 5, 8, 14-18 and 28 have been presented for reconsideration in view of Applicant's arguments. Claims 31-40 have been presented for examination.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 4, 5, 8, 14-18, 28 and 31-40 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

35 U.S.C. § 101 requires that an Applicant's invention disclose a *useful, tangible and concrete* result.

2.1 Claims 4, 5, 8, 14-18, 28 and 31-40 fail to disclose a tangible, concrete and useful result, although Applicant's specification discloses *automated design verification for large scale integrated circuits* the specification also discloses that the *verification* can be for *other finite state systems*, the current claim language teaches *verification of other finite state system*, as such the current claim language, even in light of Applicant's specification, fails to disclose a useful

Art Unit: 2123

result because there is no disclosure in either the claim language or the specification as to what the *other finite state system* would be. Further, the currently claimed limitation of *other finite system* is not tied to the actual physical world, for example, a *finite system* could be a finite state machine, which is an abstract concept and does not affect the physical world because it is a theoretical construct.

2.2 Claims 4, 5, 8, 14-18, 28 and 31-40 fail to disclose a useful concrete and tangible result. The current claim language discloses, initializing a structure and checking a structure for verifying properties expressed as assertion graph instances however, the current claim language fails to disclose any link to the physical world, manipulation of a assertion graph on a plurality of symbolic lattice domains fails to disclose or suggest any resultant output linking the verification of the circuit to the physical world. Applicant's instant amendments fail to disclose that any verification result is being presented into the real world. The current claim language fails to disclose providing a display of the resultant verification to a user as well as providing any signal or file to affect the production of the actual integrated circuit. Further, the manipulation of an assertion graph and the subsequent verification of a symbolic simulation relation is merely teaching the manipulation of an abstract concept, which is non-statutory subject matter, see section 2106.02 of the Rev. 5 Aug. 2006 revision of the MPEP.

2.3 As regards independent claim 28, the recited means under 112 6th paragraph could be interpreted to be the programmed methods as disclosed on page 35 of Applicant's specification. As such, the claimed means amounts to software only, then the claimed system is composed of functional descriptive material, which is non-statutory see section 2106.01 of the Rev. 5 Aug. 2006 revision of the MPEP.

2.4 Amendment is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4, 5, 8, 14-18, 28 and 31-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3.1 Claims 4, 5, 8, 14-18, 28 and 31-40 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: how *a formal verification of a circuit* is performed by *initialization of a symbolic simulation relation for an assertion graph on a first lattice domain*. The current claim language fails to provide a linkage between *circuit verification* and manipulation/initialization of an *assertion graph in a first symbolic lattice domain*.

3.2 Claims 4, 5, 8, 14-18, 28 and 31-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is unclear what the *metes and bounds* are of *other finite state systems*. A review of Applicant's specification has failed to provide a definition of the bounds of the phrase *other finite state system*.

3.3 Amendment is required.

Response to Arguments

4. Applicant's arguments filed 9/28/2006 have been fully considered but they are not persuasive.

4.1 Applicant argued on page 9 of the response that, "*The instant claim language when correlated with the corresponding structures and processes set forth in the specification makes it apparent to one of ordinary skill in the art that each claimed invention, respectively, has a practical application in the technical arts*", while the claims should always be considered in light of the specification, the examiner is *required* during prosecution to apply a reasonable interpretation of the claims as presented in the instant application, further the current claim language teaches manipulation of an abstract idea and is absent of any claimed practical application. While the preamble of the claim teaches the verification of a circuit, the claims are silent regarding how the claimed *symbolic simulation relation for an assertion graph* is used to verify said circuit and further how this verification is then presented into the *real-world* where the result would be *useful*. Applicant has argued that an artisan of ordinary skill, in light of the specification, would understand the practical application of the claimed subject matter, this is not the test for a claim being directed towards statutory subject matter. The claim must expressly disclose a *useful concrete and tangible* result or said claim is not directed towards statutory subject matter, see section 2106.02 of the Rev. 4 Aug. 2006 edition of the MPEP.

On page 10 Applicant argued that, "*Transformation and reduction of an article to a different state or thing is the clue to the patentability of a process claim...*" the claimed *other*

Art Unit: 2123

finite state system and the *assertion graph* are not articles; they are abstract constructs and are not tangible.

On page 11 Applicant argued that, "...*the assertion graph on the first lattice domain is configurable to express a justification property to verify the symbolic relation*", the examiner fails to see how the current claim language relates *verification of a symbolic relation* with the verification of a description of a logic circuit.

On page 11 Applicant has disclosed the support for the claimed methods, the current claims are not being rejected under 35 USC 112 1st paragraph the current claims are enabled.

Allowable Subject Matter

5. As indicated in the Office Action dated 10/5/2005 the subject matter of Applicant's claims is patentable in view of the prior art however, the currently claimed subject matter is under rejection in view of 35 U.S.C. 101 and 35 U.S.C. 112 2nd paragraph.

5.1 As regards the newly presented claims 31-40, they are allowable over the prior art for at least the reason that they depend upon allowed base claims.

Conclusion

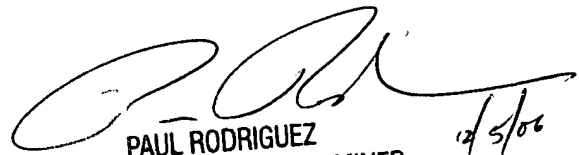
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwain M. Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

Art Unit: 2123

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dwin McTaggart Craig


PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
12/5/06